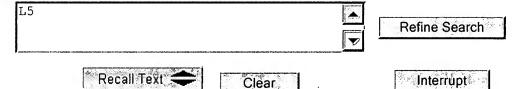
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Terms	Documents	
L4 and (PCI or "PCI Express")	54	

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<u>L5</u>	L4 and (PCI or "PCI Express")	54	<u>L5</u>
<u>L4</u>	12 same (mode or type or phase)	588	<u>L4</u>
<u>L3</u>	L2 and (PCI or "PCI Express")	249	<u>L3</u>
<u>L2</u>	(port near10 connect\$4) same (set or bunch or group) same (less or smaller or "same")	2332	<u>L2</u>
DB=D	WPI; PLUR = YES; OP = OR		
<u>L1</u>	(port near10 connect\$4) same (set or bunch or group) same (less or smaller or "same")	250	<u>L1</u>

END OF SEARCH HISTORY

Search Results -

Terms	Documents	
L7 and (PCI or "PCI Express")	123	

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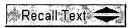
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DB=P	PGPB, USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR=YES; OP=OR		
<u>L8</u>	L7 and (PCI or "PCI Express")	123	<u>L8</u>
<u>L7</u>	l6 same (mode or type or phase)	9329	<u>L7</u>
<u>L6</u>	(port near10 connect\$4) same (set or bunch or group) same (less or smaller or "same")	25620	<u>L6</u>
DB=P	GPB; PLUR=YES; OP=OR		
<u>L5</u>	L4 and (PCI or "PCI Express")	54	<u>L5</u>
<u>L4</u>	12 same (mode or type or phase)	588	<u>L4</u>
<u>L3</u>	L2 and (PCI or "PCI Express")	249	<u>L3</u>
<u>L2</u>	(port near10 connect\$4) same (set or bunch or group) same (less or smaller or "same")	2332	<u>L2</u>
DB=D	OWPI; PLUR=YES; OP=OR		
<u>L1</u>	(port near10 connect\$4) same (set or bunch or group) same (less or smaller or "same")	250	<u>L1</u>

Search Results -

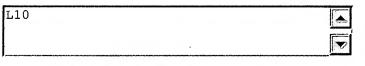
Terms	Documents		
L8 and L9	5		

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<u>L10</u> .	18 and L9	5	<u>L1</u>
<u>L9</u>	710/100,33,300-	17257	L!
	302,72,306,313;345/520,531;361/679,683,783;709/253;326/37;375/376;370/254.ccls.		
<u>L8</u>	L7 and (PCI or "PCI Express")	123	L
<u>L7</u>	l6 same (mode or type or phase)	9329	<u>L'</u>
<u>L6</u>	(port near10 connect\$4) same (set or bunch or group) same (less or smaller or "same")	25620	<u>L(</u>
DB	=PGPB; PLUR=YES; OP=OR		
<u>L5</u>	L4 and (PCI or "PCI Express")	54	<u>L.</u> '
<u>L4</u>	12 same (mode or type or phase)	588	L
<u>L3</u>	L2 and (PCI or "PCI Express")	249	<u>L:</u>
<u>L2</u>	(port near10 connect\$4) same (set or bunch or group) same (less or smaller or "same")	2332	<u>L:</u>

DB=DWPI; PLUR=YES; OP=OR

L1 (port near10 connect\$4) same (set or bunch or group) same (less or smaller or "same")

250 <u>L</u>:

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Search Results -

Terms	Documents	
L1 and L3	308	

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<u>L4</u>	11 and L3	308	<u>L4</u>
<u>L3</u>	L2 and (card or board or motherboard)	30455	<u>L3</u>
<u>L2</u>	(port near10 connect\$4) same (mode or type or phase)	106141	<u>L2</u>
<u>L1</u>	710/14,106,107,305,311;370/351.ccls.	5686	<u>L1</u>

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SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip]

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HiBRID-SoC: a system-on-chip architecture with two multimedia DSPs

and a RISC core

Friebe, L. Stolberg, H.-J. Berekovic, M. Moch, S. Kulaczewski, M.B. Dehnhardt, A. Pirsch, R. Inst. fur Mikroelektronische Syst., Hannover Univ., Germany

This paper appears in: SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip] Publication Date: 17-20 Sept. 2003

On page(s): 85 - 88

Number of Pages: 427

Posted online: 2003-11-03 15:50:00.0 INSPEC Accession Number:7816081

between the cores. The HiBRID-SoC is fabricated in a 0.18 /spl mu/m 6LM standard-cell technology, occupies Flash, and host system access are connected via a 64 bit AMBA AHB system bus with the processor cores. algorithms, and the stream processor for bitstream processing. Dedicated interface units for SDRAM, serial The HiBRID-SoC integrates three fully programmable processor cores, each optimized towards a particular class of algorithm: the HiPAR-DSP for DSP oriented functions, the macroblock processor for block oriented Dual-**port** memories between the processor cores facilitate fast data and control information exchange about 82 mm/sup 2/, and operates at 160 MHz.

Index Terms Inspec

Controlled Indexing

digital signal processing chips integrated circuit design logic design multimedia computing reduced instruction set computing system buses system-on-chip

Non-controlled Indexing

0.18 micron 160 MHz 64 bit ARB system bus interface DSP oriented functions HiBRIDinformation exchange data information exchange dual-port memories fully programmable processor cores host system access macroblock processor multimedia DSP multimedia signal processing applications serial Flash stream processor system-on-chip architecture SoC RISC core SDRAM SoC bitstream processing block oriented algorithms control

Author Keywords Not Available